OIPE JC106
MAY 02 2005
PATENT & TRADEMARK OFFICE

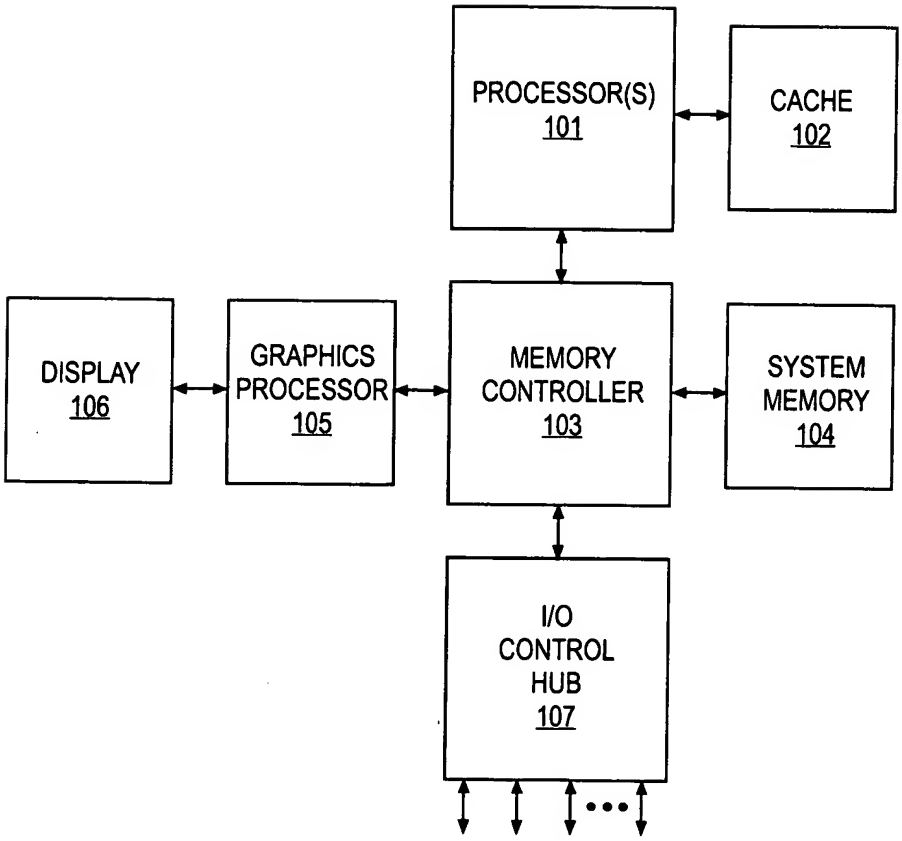

FIG. 1
(PRIOR ART)

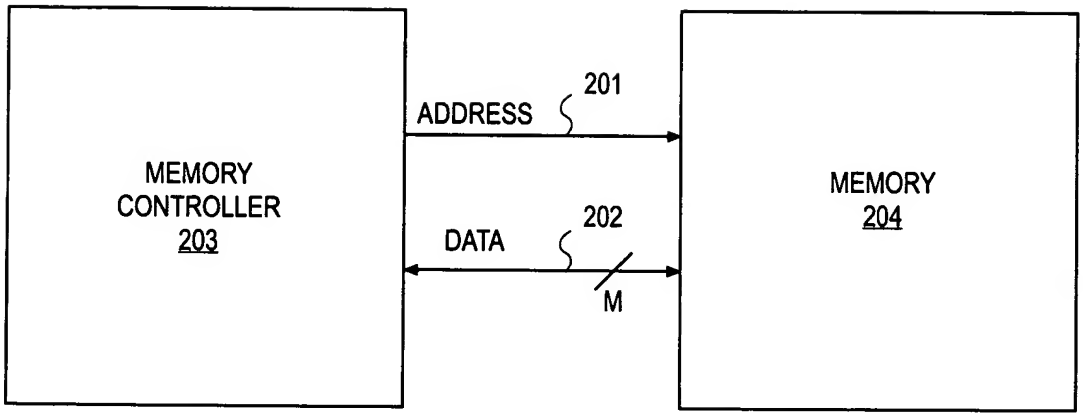

FIG. 2
(PRIOR ART)

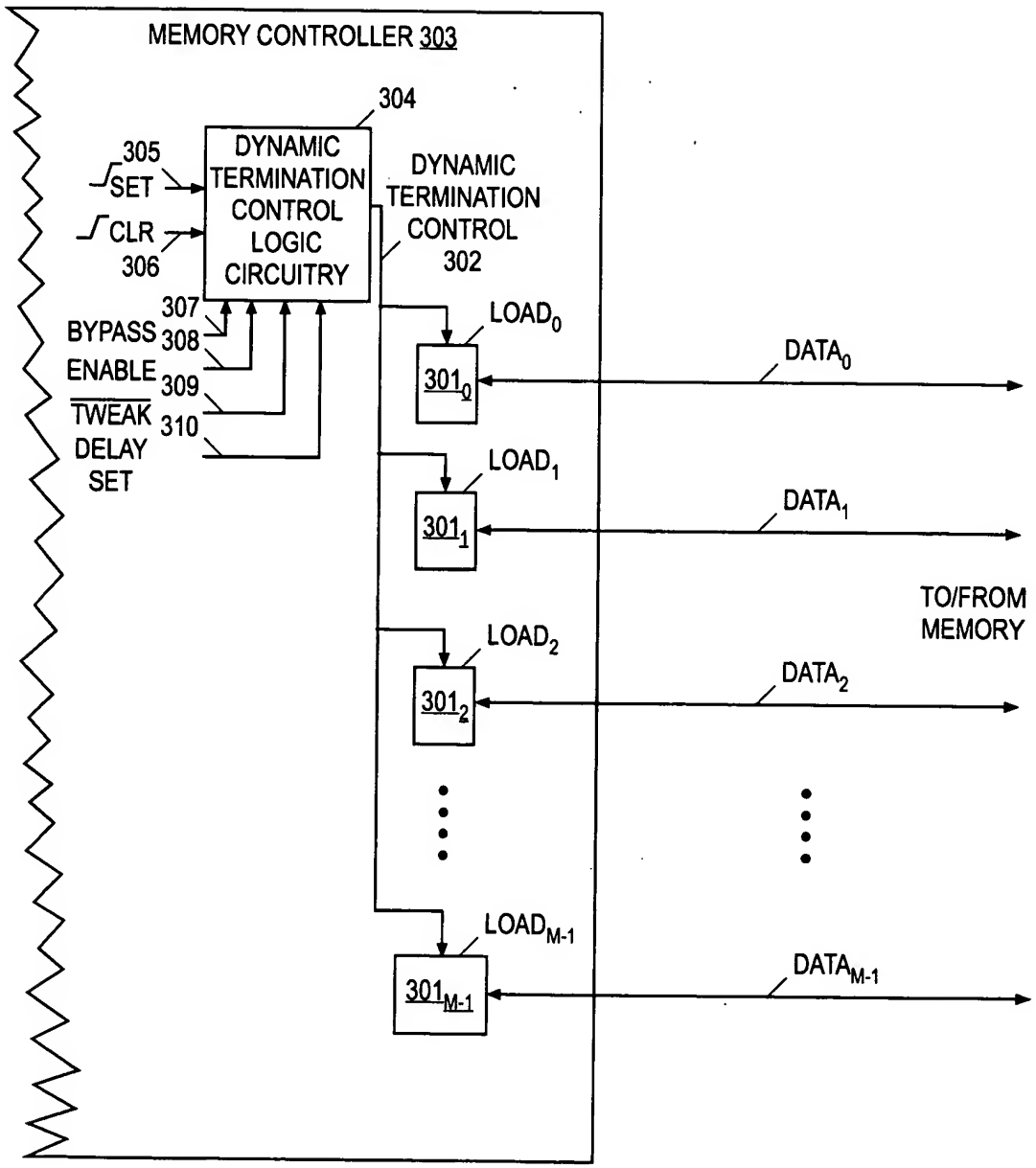

FIG. 3

311

MEMORY FUNCTION	WRITE	READ
LOAD IMPEDANCE S.T.	INACTIVE	ACTIVE

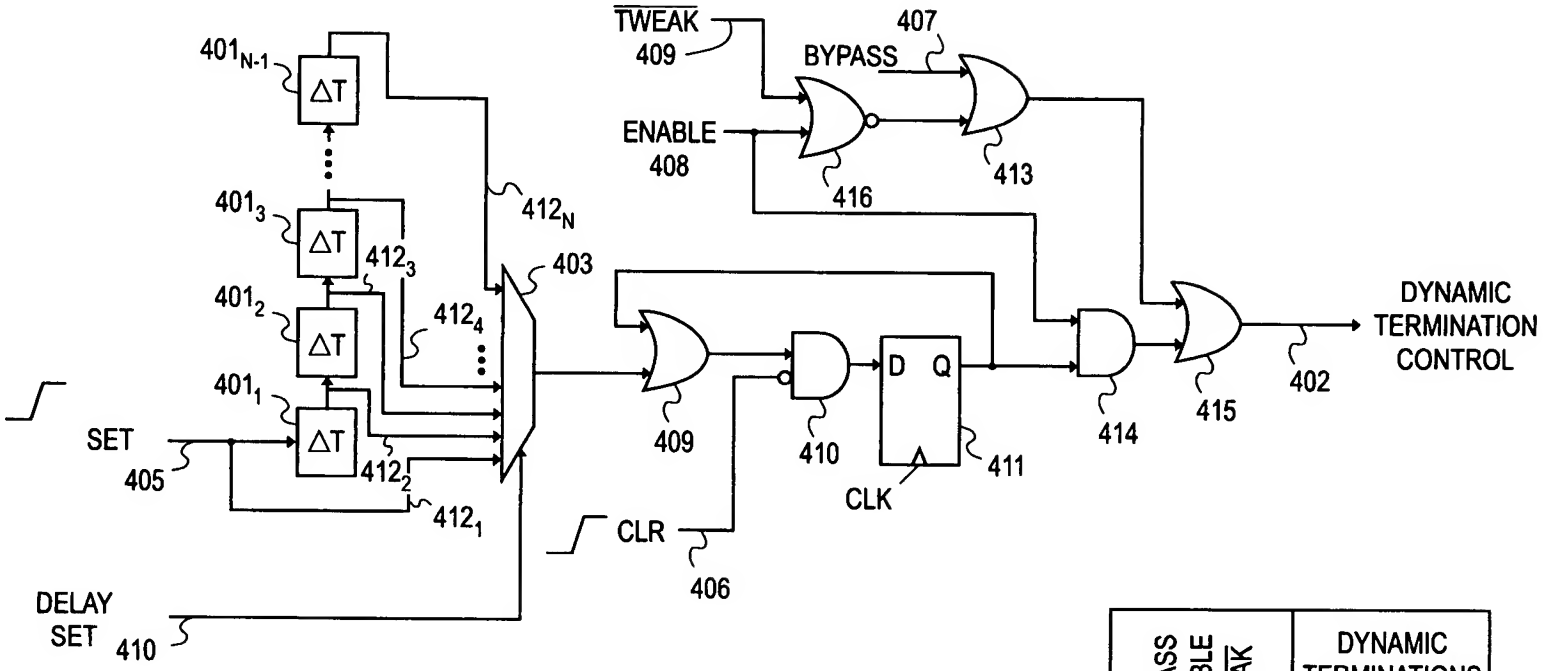

FIG. 4

BYPASS	ENABLE	$\overline{\text{TWEAK}}$	DYNAMIC TERMINATIONS CONTROL	
H	X	X	H	← 420
L	H	X	Q	← 421
L	L	L	H	} 422
L	L	H	L	

419

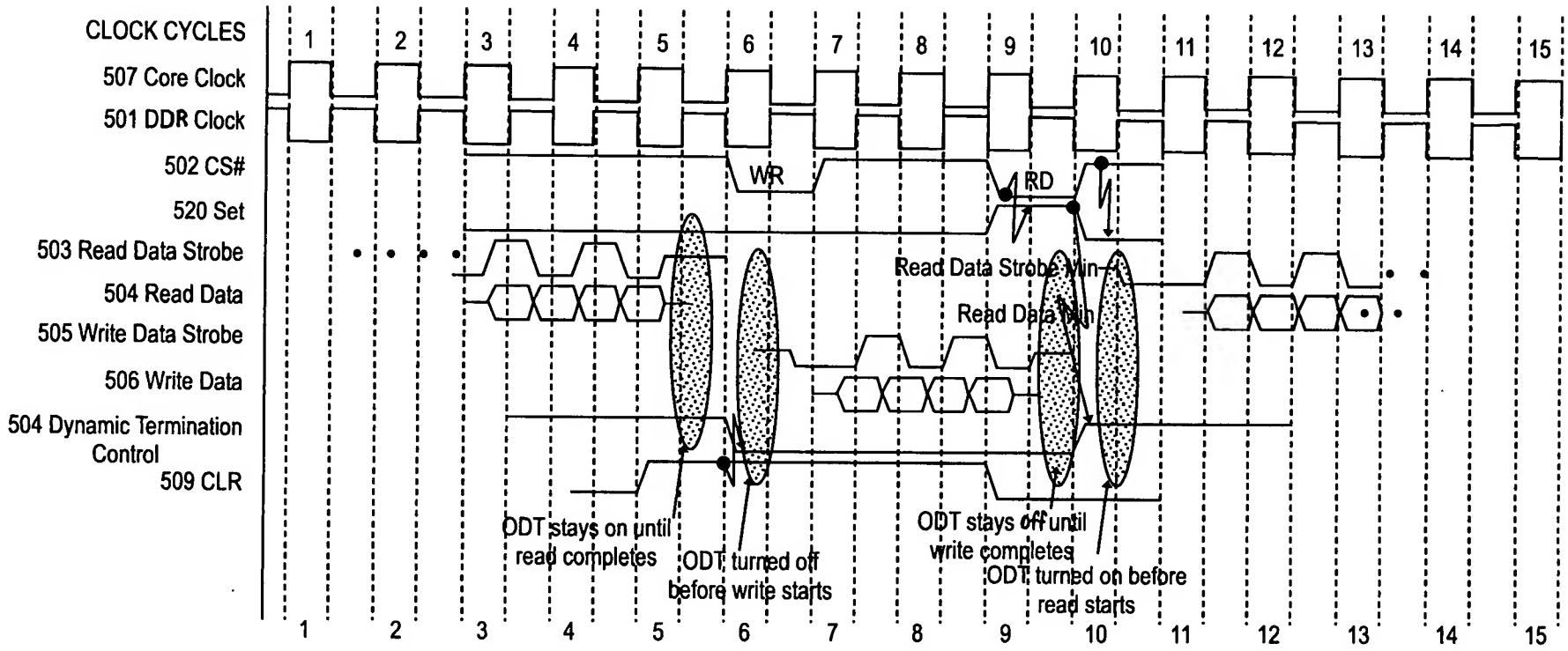
CLOCK CYCLES
507 Core Clock
501 DDR Clock
502 CS#
520 Set
503 Read Data Strobe
504 Read Data
505 Write Data Strobe
506 Write Data
504 Dynamic Termination Control
509 CLR
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
WR
RD
Read Data Strobe Min
Read Data Min
ODT stays on until read completes
ODT turned off before write starts
ODT stays off until write completes
ODT turned on before read starts

FIG. 5

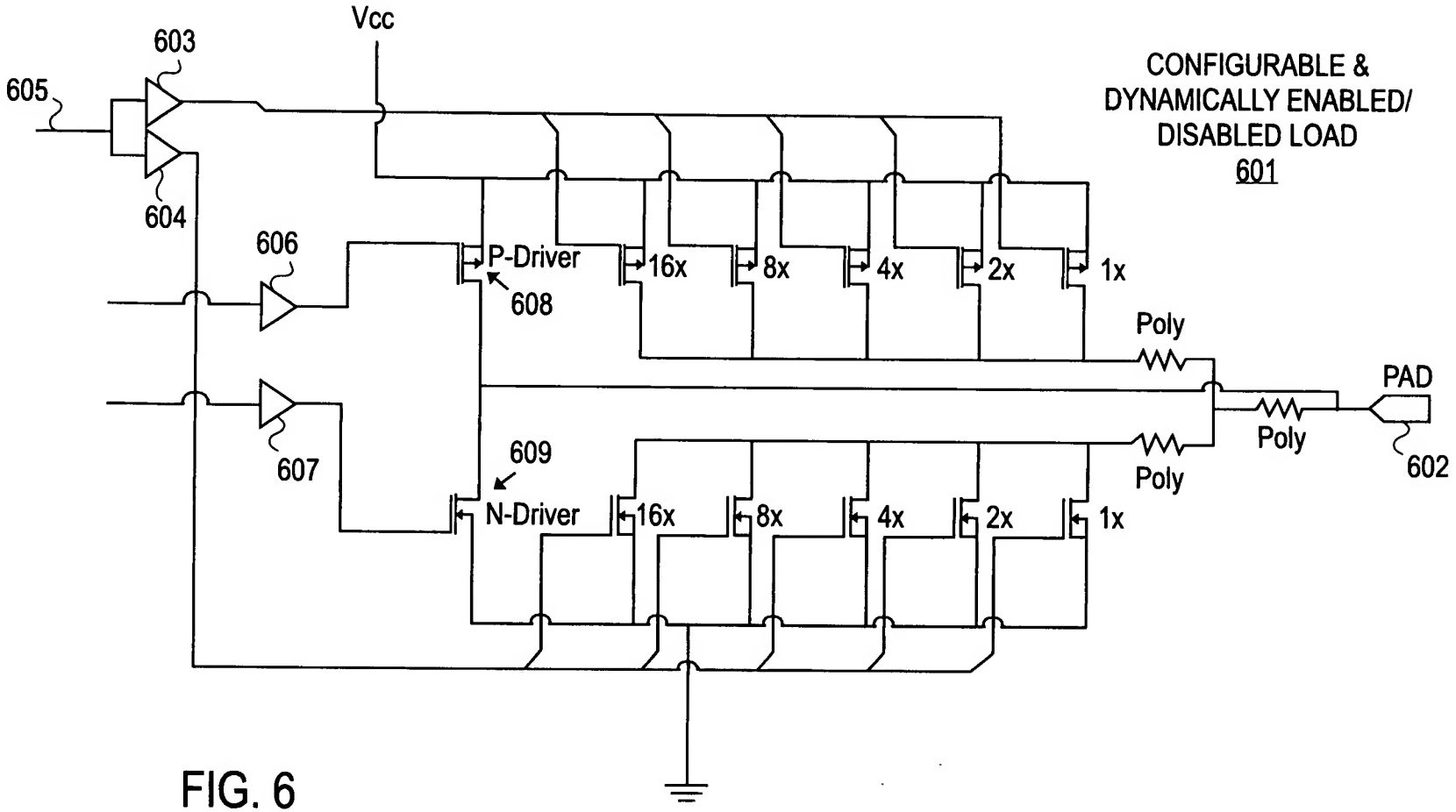
Vcc
603
605
604
606
607
608
609
P-Driver
N-Driver
16x
8x
4x
2x
1x
CONFIGURABLE &
DYNAMICALLY ENABLED/
DISABLED LOAD
601
Poly
Poly
Poly
PAD
602

FIG. 6